

## IN THE CLAIMS

Please amend claims 1, 2, 6, 8, 9, 14, and 17 as follows. All claims have been provided as a courtesy to the Examiner.

1 1. (Twice Amended) A memory module, comprising:  
2 a plurality of memory devices; and  
3 a memory module controller [configured] to receive a first memory transaction in a  
4 first format from a first memory bus, and to convert the first memory transaction into a  
5 second memory transaction in a second format for the plurality of memory devices, the  
6 second format of the second memory transaction being different from the first format of the  
7 first memory transaction.

1 2. (Twice Amended) The memory module of claim 1, wherein the memory module  
2 controller is [also configured] to reformat the first memory transaction in the first format  
3 into the second memory transaction in the second format, and is to provide the second  
4 memory transaction to at least one of the plurality of memory devices.

1 3. (Unchanged) The memory module of claim 1, further comprising:  
2 a second memory bus coupled between the memory module controller and the  
3 plurality of memory devices.

1 4. (Unchanged) The memory module of claim 3, wherein the second memory bus  
2 comprises separate address, data, and control signal lines.

1 5. (Unchanged) The memory module of claim 3, wherein the second memory bus  
2 comprises a signal line for a clock signal.

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B2 1 6. (Twice Amended) The memory module of claim 3, wherein the first memory  
2 bus is to operate [operates] at a first data rate and the second memory bus is to operate  
3 [operates] at a second data rate, and wherein the first data rate is different than the second  
4 data rate.

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1 7. (Unchanged) The memory module of claim 1, wherein the first memory bus  
2 includes a first number of signal lines and the second memory bus includes a second  
3 number of signal lines, and wherein the first number is different than the second number.

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B3 1 8. (Twice Amended) The memory module of claim 1, wherein the memory module  
2 controller comprises:  
3 request handling circuitry [configured] to receive the first memory transaction from  
4 the first memory bus; and  
5 control logic coupled to the request handling circuitry and [configured] to reformat  
6 the first memory transaction and to provide the reformatted first memory transaction to at  
7 least one of the plurality of memory devices.

1 9. (Twice Amended) The memory module of claim 1, wherein the first memory  
2 bus is [configured] to carry time-multiplexed data and address information, and the second  
3 memory bus includes separate address and data lines.

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1 10. (Unchanged) The memory module of claim 1, wherein the memory module is a  
2 dual in-line first memory module (DIMM).

1 11. (Unchanged) The memory module of claim 1, wherein the memory module is a  
2 single in-line first memory module (SIMM).

1 12. (Unchanged) The memory module of claim 1, wherein the plurality of memory  
2 devices comprise volatile memory devices.

1 13. (Unchanged) The memory module of claim 1, wherein the plurality of memory  
2 devices comprise nonvolatile memory devices.

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1 14. (Twice Amended) The memory module of claim 1, wherein the memory module  
2 controller is [configured] to generate a handshake signal that indicates [when] if the  
3 memory module controller is communicating data to the system memory controller.

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1 15. (Unchanged) The memory module of claim 1, wherein the first memory  
2 transaction is a write transaction.

1 16. (Unchanged) The memory module of claim 1, wherein the first memory  
2 transaction is a read transaction.

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1 17. (Twice Amended) A memory module, comprising:  
2 a plurality of memory devices; and  
3 a memory module controller coupled to the plurality of memory devices, the  
4 memory module controller [being configured] to receive a first memory transaction in a  
5 first format from a memory bus, and to convert the first memory transaction into a second  
6 memory transaction in a second format, and to provide the second memory transaction in  
7 the second format to at least one of the plurality of memory devices.

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